IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: DEBASHIS BHATTACHARYA

Serial No.:   09/896,071

Filed: JUNE 29, 2001

For: PROCESS FOR AUTOMATED GENERATION OF DESIGN-SPECIFIC COMPLEX FUNCTIONAL BLOCKS TO IMPROVE QUALITY OF SYNTHESIZED DIGITAL INTEGRATED CIRCUITS IN CMOS

Art Unit: 2825
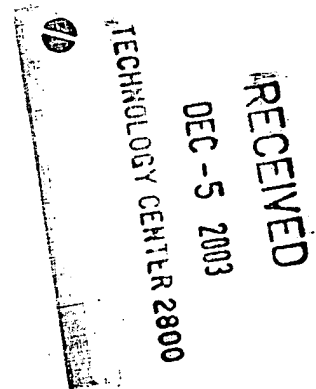
Examiner: DO, THUAN V.

Confirmation No.:   9529
Customer No.:   27623
Attorney Docket: 162.7106USU

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Sir:

In reply to the non-final Office Action dated June 19, 2003, for which the time for a response has been extended two (2) months to include November 19, 2003, please amend the above patent application as follows:

Amendments to the Claims begin on page 2 of this paper.
Remarks begin on page 8 of this paper.

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